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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,611	02/05/2004	Hiroyuki Senda	YAO-4210US1	5071
23122	7590	10/18/2005	EXAMINER	
RATNERPRESTIA			TORRES, JOSEPH D	
P O BOX 980			ART UNIT	
VALLEY FORGE, PA 19482-0980			PAPER NUMBER	
			2133	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/772,611

Applicant(s)

SENDA ET AL.

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 41 and 42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 41 and 42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/311,394.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 09/12/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Applicants pointed out that the contents of Flip-Flops D1 and D2 are referred as "the internal states" (Applicants also referred the Examiner to Fig. 7). Therefore, in Fig. 7, for example, the trellis-encoded signal has 4 internal states, or 2^S (i.e., $S=2$), represented by S^0 to S^3 , whereby $D1D2 = 00, 01, 10, \text{ and } 11$ ".

The Examiner disagrees and asserts that the output of trellis encoded signal Z0, Z1 in Figures 6 and 7 of the Applicant's disclosure depends on the input value Y1 and state values D0 and D1, but generally do not take on the state values (Note: Y1 in Figure 6 equals R in Figure 7 and Z0, Z1 in Figures 6 equals Y2 and Y1 in Figure 7). For Example if $Y1=+3$ and $D0 D1 = 01$ then $Z0Z1=10$ and if $Y1=+3$ and $D0 D1 = 11$ then $Z0Z1=10$ in Figure 7 (Note: Y2 and Y1 in Figure 7, i.e., Z0 and Z1 in Figures 6, are output values of the state machine D0 and D1 in Figure 6 or output values assigned to branches of the State Diagram in Figure 7 and are not the states D0 D1 of the state machine D0 and D1 in Figure 6 nor states D0 D1 of the State Diagram in Figure 7). The only thing that the Applicant teaches is a trellis-encoded signal generated by a state machine having 4 internal states, not a trellis-encoded signal having 4 internal states. The Trellis encoded signal is a signal made up of symbols generated by a state

machine having 4 internal states and the symbols that make up the Trellis-encoded signal are not states. If the Applicant disagrees and believes that the Applicant is correct, then surely the Applicant must be able to write down an example of a Trellis encoded signal $s=(s_1, s_2, s_3, \dots)$ comprising symbols s_1, s_2, s_3, \dots whereby each symbol is a particular value Z0 Z1 in Figure 6 generated by the state machine D0 D1 showing how the symbols s_1, s_2, s_3, \dots make up states D0 D1 of a state machine. **The Examiner requests that the Applicant do so, i.e., demonstrate by example a Trellis encoded signal $s=(s_1, s_2, s_3, \dots)$ comprising symbols s_1, s_2, s_3, \dots whereby each symbol is a particular value Z0 Z1 in Figure 6 generated by the state machine D0 D1 showing how the symbols s_1, s_2, s_3, \dots make up states D0 D1 of a state machine, providing support in the Applicant's specification.** Note: Y2 and Y1 in Figure 7, i.e., Z0 and Z1 in Figures 6, are output values of the state machine D0 and D1 in Figure 6 or output values assigned to branches of the State Diagram in Figure 7 and are not the states D0 D1 of the state machine D0 and D1 in Figure 6 nor states D0 D1 of the State Diagram in Figure 7. Hence, the trellis encoded signal Z0, Z1 in Figure 6 or Y2 and Y1 in Figure 7 of the Applicant's disclosure do not have states.

The Applicant contends, "In particular, the Flu Patent eludes to disclosing that regardless of whether a 4-state or 8-state trellis-encoded signal is received, the received signal is decoded using an 8-state transition diagram, and not a 4-state transition diagram as would be the case in Applicants' claimed invention. Most specifically, the Fu Patent states that "in the filter mode when transition filter 22 is used,

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an eight trellis decoder is required, and in the non-filtered mode when filter 22 is not used, a four state trellis decoder is required, as known”.

The Examiner would like to point out that the Examiner is treating the last limitation “decoding the converted signal using the state transition diagram having 2^s internal states” in claims 41 and 42 as a typographical error and assuming --decoding the converted signal using the state transition diagram having 2^{s+1} internal states-- was intended since that is what the Applicant teaches (lines 19-23 on page 50 of the Applicant’s disclosure). The Examiner would also like to point out that it makes no sense to convert a signal encoded by a state machine having 2^s states to mimic a signal encoded by a state machine having 2^{s+1} states to then decode it using a state transition diagram having 2^s states since the original signal could have been just as easily decoded using the state transition diagram having 2^s states without having to be converted. Besides that nowhere does the Applicant teach how to decode a signal encoded by a state machine having 2^{s+1} states using a state transition diagram having 2^s states. The Examiner doubts the Applicant intended “decoding the converted signal using the state transition diagram having 2^s internal states” [Emphasis Added], unless the Applicant was purposely trying to create a device to bog down communications with extra calculations.

The Examiner disagrees with the applicant and maintains all rejections of claims 41 and 42. All amendments and arguments by the applicant have been considered. It is the Examiner’s conclusion that claims 41 and 42 are not patentably distinct or non-obvious

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over the prior art of record in view of the reference, Hu; Keren et al. (US 5838729 A, hereafter referred to as Hu) as applied in the last office action, filed 06/08/2005.

Therefore, the rejection is maintained.

Specification

The objection below was copied from the previous office Action without any changes.

2. The disclosure is objected to because of the following informalities: Claims 41 and 42 recite, "the received trellis-encoded signal having 2^s internal states". Nowhere in the specification does the Applicant teach a signal having 2^s internal states.

Claims 41 and 42 recite, "a signal having $2^{(s+1)}$ internal states". Nowhere in the specification does the Applicant teach a signal having $2^{(s+1)}$ internal states.

The Examiner asserts that that a trellis-encoded signal is a signal generated from encoded binary data that was encoded using an N-state state machine. If that is what the Applicant intends, the Applicant should rewrite the claims to reflect that interpretation.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The rejections below were copied from the previous office Action without any changes.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

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The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 41 and 42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 41 and 42 recite, "the received trellis-encoded signal having 2^s internal states". Nowhere in the specification does the Applicant teach a signal having 2^s internal states.

Claims 41 and 42 recite, "a signal having $2^{(s+1)}$ internal states". Nowhere in the specification does the Applicant teach a signal having $2^{(s+1)}$ internal states.

The Examiner asserts that that a trellis-encoded signal is a signal generated from encoded binary data that was encoded using an N-state state machine. If that is what the Applicant intends, the Applicant should rewrite the claims to reflect that interpretation.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 41 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 41 and 42 recite, “the received trellis-encoded signal having 2^s internal states”, which does not make sense. Claims 41 and 42 recite, “a signal having $2^{(s+1)}$ internal states”, which does not make sense. The Examiner asserts that that a trellis-encoded signal is a signal generated from encoded binary data that was encoded using an N-state state machine. If that is what the Applicant intends, the Applicant should rewrite the claims to reflect that interpretation.

Claims 41 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claims 41 and 42 recite, “the received trellis-encoded signal having 2^s internal states”. Claims 41 and 42 recite, “a signal having $2^{(s+1)}$ internal states”. The omitted structural cooperative relationships are: the relationship between a “signal” and “internal states” of a state machine.

Claim Rejections - 35 USC § 102

The rejection below was copied from the previous office Action highlighting newly added comments used to address arguments in the Applicant’s response underlined bold.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Hu; Keren et al. (US 5838729 A, hereafter referred to as Hu).

Col. 8, lines 23-34 in Hu teaches that an 8 state ACS architecture is used to decode both binary data encoded using an 8-state state machine and binary data encoded using an 4-state state machine. That is: the 8 state ACS architecture is used to decode binary data encoded using an 4-state state machine by treating the binary data encoded using an 4-state state machine as binary data encoded using an 8-state state machine to emulate 4 state ACS architecture to decode the binary data encoded using an 4-state state machine based on a 4 state trellis diagram.

The Examiner would like to point out that the Examiner is treating the last limitation “decoding the converted signal using the state transition diagram having 2^s internal states” in claims 41 and 42 as a typographical error and assuming --decoding the converted signal using the state transition diagram having 2^{s+1} internal states-- was intended since that is what the Applicant teaches (lines 19-23 on page 50 of the Applicant’s disclosure). The Examiner would also like to point out that it makes no sense to convert a signal encoded by a state machine having 2^s states to mimic a signal encoded by a state machine having 2^{s+1} states to then decode it using a state transition diagram having 2^s states since the original signal could have been just as easily decoded using the state transition diagram having 2^s states without having to be converted. Besides that

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nowhere does the Applicant teach how to decode a signal encoded by a state machine having 2^{s+1} states using a state transition diagram having 2^s states. The Examiner doubts the Applicant intended “decoding the converted signal using the state transition diagram having 2^s internal states” [Emphasis Added], unless the Applicant was purposely trying to create a device to bog down communications with extra calculations.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
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